ABSTRACT

In parallel with accesses to a cache made by a core processor, a DMA controller is used to pre-load data from a main memory into the cache. In this manner, the pre-load function can make the data available to the processor application before the application references the data, thereby potentially providing a 100% cache hit ratio since the correct data is pre-loaded into the cache. In addition, if a copy-back cache is employed, the cache memory system can also be configured such that processed data can be dynamically unloaded from the cache to the main memory in parallel with accesses to the cache made by the core processor. The pre-loading and/or post unloading of data may be accomplished, for example, by using a DMA controller to burst data into and out of the cache in parallel with accesses to the cache by the core processor. This DMA control function may be integrated into the existing cache control logic so as to reduce the complexity of the cache hardware (e.g., as compared to a multi-port cache), and to alleviate the difficulty associated with addressing the non-contiguous internal address map of the cache. By employing a DMA controller having flexible address generation and transfer control capabilities, data can be transferred from an atypical memory-mapped entity (e.g., a FIFO buffer of a peripheral) directly to the cache.